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ABSTRACT

This report showcases a vertical tunnel field effect transistor (TFET) fabricated from a GaN/InGaN heterostructure and compares it to a gated vertical GaN p-n diode. By including a thin InGaN layer, the interband tunneling in the TFET is increased compared to the gated homojunction diode. This leads to an increased drain current of 57 μA/μm and a reduced subthreshold swing of 102 mV/dec, from 240 mV/dec. However, trap assisted tunneling prevents devices from realizing subthreshold slopes below the Boltzmann limit of 60 mV/dec. Nevertheless, this work shows the capability of tunnel field effect transistors to be realized in GaN by taking advantage of the spontaneous and piezoelectric polarization in the III-N material system.

Due to the thermally restricted subthreshold swing (SS) of 60 mV/dec at room temperature, current state-of-the-art field-effect transistors (FETs) including complementary metal-oxide-semiconductor (CMOS) technology are unable to lower supply voltage without creating unacceptable levels of static power consumption. An alternative for low voltage logic is the tunnel field effect transistor (TFET).[1] By taking advantage of interband tunneling between the source and channel, TFETs filter out the high energy electrons that limit the SS in CMOS. Through proper device design, a SS lower than 60 mV/dec at room temperature can be achieved. Indeed, this has been seen in Si,[2,3] Ge,[4] III–V,[5–7] and 2D[8] material systems.

However, TFETs based on small bandgap materials suffer from large off state leakage current, due to ambipolar current conduction.[9] While methods for minimizing this current have been investigated,[10] use of a wide bandgap semiconductor would greatly suppress it. By employing a heterostructure, the dual requirements of high on current and low off current could be realized in the resulting TFET.

A promising group of materials capable of suppressing ambipolar leakage while at the same time breaking the fundamental thermionic limit is the III-nitride semiconductor system. Consisting of GaN, InN, and AlN, this semiconductor family has shown considerable promise in the areas of high-frequency and power electronics,[11] visible[12] and UV LEDs,[13] and interband[14] and intraband[15,16] tunneling devices. With GaN's wide bandgap of 3.4 eV, it is also a promising semiconductor material for low leakage TFETs, required in low-power digital logic applications.[17]

In this report, the built-in polarization fields within III-nitride heterostructures are exploited to demonstrate a nitride TFET. The proposed device structure can be seen in Fig. 1(a). While Off, the wide bandgap of GaN prevents ambipolar leakage current, which is a major advantage over narrow bandgap semiconductor heterostructures. However, this benefit also prevents efficient interband coupling between the conduction and valence electronic states. In traditional semiconductors, impurity[18,19] and electrostatic doping[20] are sufficient to establish intense electric fields (~0.5 MV/cm), which enable interband tunneling transport. In contrast, because of their wider bandgaps, III-nitride heterostructures require stronger electric fields which are difficult to attain by impurity doping due to the low p-type ionization efficiency.[21] In this scenario, the intense spontaneous and piezoelectric polarization fields are leveraged to engineer internal electric fields with intensities on the order of ~6 MV/cm and are capable of enabling interband tunneling

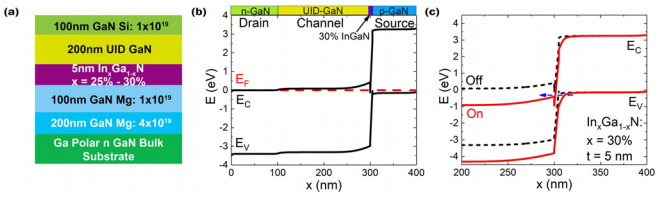

FIG. 1. (a) Heterostructure design of the proposed TFET. All doping densities are in cm^{-3} Ohmic contact to p-GaN is achieved through backside interband tunneling at the p-GaN growth interface. (b) Equilibrium energy band diagram of structure proposed in (a). Due to the inclusion of the InGaN layer, the field at the p-GaN/UID GaN interface in significantly enhanced. (c) Comparison of On and Off states for a GaN TFET. By applying a large enough gate field, a type III band alignment is achieved, enabling interband tunneling of electrons from the source to the channel.

injection.[22–24] As can be seen in Figs. 1(b) and 1(c), inclusion of the thin InGaN layer breaks the translation symmetry of the atomic dipole distribution, resulting in a strong electrostatic polarization within the InGaN layer, which enhances the built-in field of the p-n junction. When this structure is biased in the On state, the small bandgap and lower effective mass of InGaN, combined with the polarization-induced electric fields, result in an exponential enhancement of the tunneling transmission from the valence band of the source to the conduction band of the channel, creating a substantial On-current.

Simulations by Li *et al.*[25,26] predicted that a GaN/InN/GaN nanowire TFET is capable of achieving a SS as low as 15 mV/dec, with saturation currents near 100 $\mu A/\mu m$. We recently reported the first experimental implementation of the GaN TFET enabled by polarization engineering.[27] The device presented was able to achieve current densities of 10 $\mu A/\mu m$ with a SS of 109 mV/dec. The goal of this report is to elaborate on the design, fabrication, and operation of the nitride TFET, by comparing it to a gated vertical GaN p-n homojunction of similar geometry.

Two different devices are investigated: a vertical gated p-n junction and a vertical TFET. Figures 2(a) and 2(b) show the two device geometries, and the corresponding layers of each device. The p-n diode and TFET were fabricated on single crystal n^+ Ga-polar GaN substrates from Ammono and Lumilog, respectively. The epitaxial growth of the layer structures of the p-n junction and TFET were performed using plasma assisted molecular beam epitaxy (MBE). Growth began with

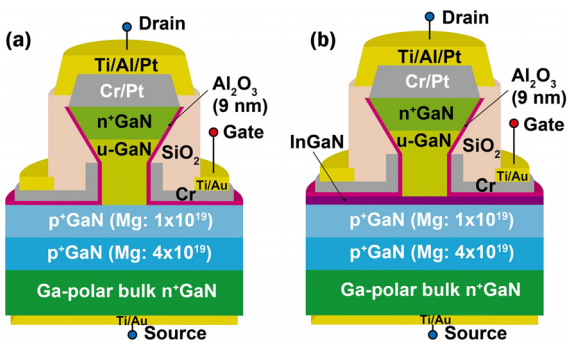

FIG. 2. Representative layouts of the two devices: (a) gated p-n diode, and (b) GaN TFET. The golf tee shape is a by-product of AZ400k wet etch. Precise control of the etch depth in the TFET is crucial for device performance.

direct nucleation of the buried p-GaN source on the substrate. 100 nm of GaN with a Mg concentration of $4 \times 10^{19}\ cm^{-3}$ was grown followed by 100 nm of GaN with a Mg concentration of $1 \times 10^{19}\ cm^{-3}$. Growth of the p-n diode continued with 200 nm of unintentionally doped (UID) GaN and finished with 100 nm of n^+-GaN, with a Si concentration of $1 \times 10^{19}\ cm^{-3}$ for the drain. The TFET structure followed the same growth as the p-n junction, but a 7 nm InGaN interlayer composed of $In_{0.27}Ga_{0.73}N$ was grown between the UID GaN and p-GaN. Group III metal, donor (Si), and acceptor (Mg) fluxes were provided by separate effusion cells, while a RF plasma source provided the active N. The TFET studied here used an InGaN layer with a 27% In content, which is predicted to produce an on current of 3 $\mu A/\mu m$.[28]

Following the epitaxial growths, the nanowires were fabricated using a two-part dry-wet etch process.[29] Immediately following the etching step, atomic layer deposition (ALD) of Al_2O_3 was used to achieve a conformal 9 nm gate oxide around the nanowires and the planar surfaces of both structures as indicated in Fig. 2. Backside p-GaN contacts were made using interband tunnel contacts, taking advantage of the highly doped bulk GaN substrate growth interface and the far larger cross-sectional area than the nanowire active regions, similar to buried tunnel-junction light emitting diodes that were demonstrated recently.[30] The 150 nm Cr/Pt etch mask was also used as the top drain contact metallization. Final drain contact pads were achieved through lift off of a sputtered Ti/Al/Pt metal stack.

The completed devices are all vertical nanowires with diameters of 380 nm for the PN diode and 470 nm for the TFET. Each device is also composed of a varying amount of wires, with the TFET containing five wires, and the diode having 400 wires. These devices were chosen as they showed the lowest gate leakage current for each device structure. A scanning electron microscope (SEM) bird's-eye image of a completed III-nitride TFET comprising five nanowires can be seen in Fig. 3(a). On the left is the drain contact pad, and on the right is the exposed gate contact pad. A close up view of the wire device is seen in Fig. 3(b), showing the complete coverage of the sputtered drain metal. For all measurements, the back-side source contacts were electrically grounded, and the voltages discussed next were applied to the top drain contacts. Current densities were calculated by normalizing measured currents to the total nanowire perimeter.

To test the junction properties, floating gate measurements were first performed. Figure 4 shows the linear and logarithmic scale current vs voltage I–V of the p-n diode [Fig. 4(a)] and the TFET [Fig. 4(b)]. For the p-n diode, behavior[31] expected from a GaN p-n diode is observed, with a turn-on voltage of 3 V, close to the bandgap of GaN. A turn-on voltage smaller than the p-n diode is measured in the TFET [Fig. 4(b)] which most likely arises from the threading dislocations in the UID GaN layer (discussed later). However, strong rectifying behavior is obtained, similar to the gated p-n junction. These results

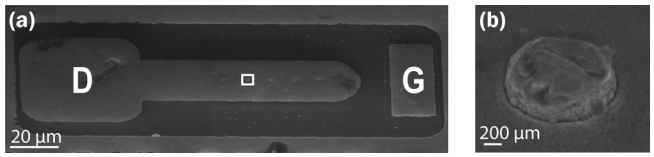

FIG. 3. (a) Bird's eye view SEM image of a fully processed single nanowire device. 200 nm of SiO_2 separates the drain metal from the gate metal. The source is not seen as it is on the backside. (b) Close up of the boxed region in (a).

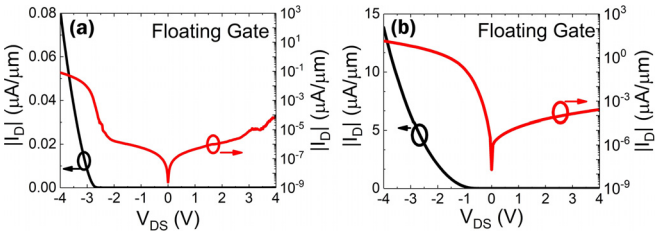

FIG. 4. Linear and semilog plots of floating gate I–V measurements for each device. (a) The gated diode shows a sharp turn on around 3 V and an On/Off ratio of three orders. (b) TFET measurements show a lower expected turn on at 2.2 V. However, the device still achieves a five order On/Off ratio, higher than that of the gated diode.

indicate that despite the lateral depletion in the UID GaN channel due to the gate, the desired p-n junction properties were preserved through processing.

The measured common-source $I_D - V_{DS}$ curves for various gate voltages for each device are shown in Fig. 5. Strong current modulation of the p-n junction currents is seen in Figs. 5(a) and 5(b). When the gate voltage is zero, an expected p-n junction I–V curve is measured with a turn-on in the negative voltage direction, and a 10^6 lower reverse current in the positive V_{DS} direction. This current–voltage characteristic of the p-n junction is found to be strongly modulated by the gate in the expected manner. Positive gate biases between 0 V → 3 V shift the turn-on voltage of the PN diode from 2.9 V toward 1.4 V. For gate voltages greater than +2 V, an interband tunneling window is opened between the valence band of the p-source and the conduction band of the n-drain similar to the current conduction in a TFET, albeit with a much larger bandgap (3.4 eV), and a far longer tunneling distance. This should lead to a low tunneling current. This gate-induced

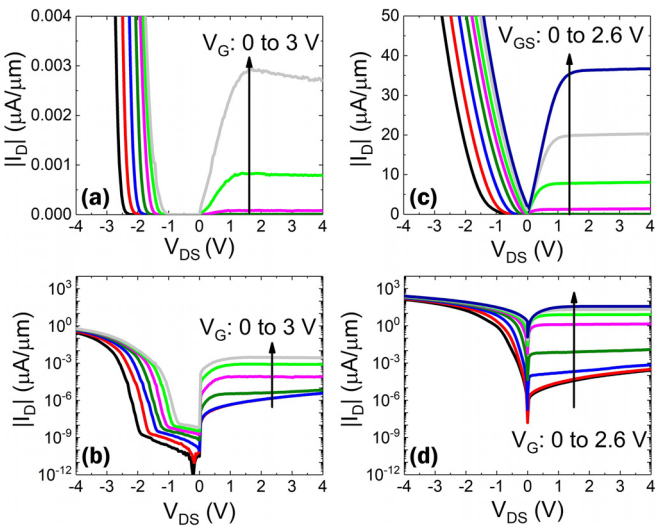

FIG. 5. Output characteristics for each device. (a) and (b) Gated p-n diode structure also shows strong charge modulation for voltages beyond 2 V, yet self-heating causes a reduction in drain current. (c) and (d) Finally, the TFET output characteristics show flat plateaus resulting in high output resistance. This behavior separates the TFET from the MOSFET.

interband tunneling current is observed as shown in Figs. 5(a) and 5(b) for positive V_{DS} values.

The measured TFET family curves are shown in Figs. 5(c) and 5(d). For positive V_{DS} voltages, good transistor behavior is observed, with current saturation and gate modulation. A saturation current of 36 μA/μm is achieved for a gate voltage of 2.6 V. For drain voltages (V_{DS}) greater than 1 V, an almost perfect saturation of current is seen in Fig. 5(c). As V_{DS} increases, the electron concentration in the channel begins to deplete, increasing the channel resistance. After the drain fully depletes the channel, any excess V_{DS} is dropped entirely across the drain/channel junction. This results in a strong current saturation.[32] For negative V_{DS} values for the TFET, the internal p-n junction is forward biased. In an ideal TFET, this current should be low, and if the p-n junction is degenerately doped, a negative differential resistance (NDR) should be visible due to Esaki tunneling. However, a NDR is not expected in the n-GaN/InGaN/p-GaN TFET active region because the junction is not degenerately doped. Thus, although the negative voltage characteristics of the TFET in Figs. 5(c) and 5(d) seem similar to a MOSFET (which has no p-type layer), a fairer comparison of the measured TFET behavior is with a gated p-n junction. This comparison indicates that for a positive V_{DS}, an interband tunneling current several orders of magnitude higher is achieved due to the polar InGaN layer inserted at the junction, with clearly observed current saturation.

The transfer curves of the two devices are shown in Fig. 6, along with their corresponding subthreshold swings. The transfer curve of the gated p-n diode, shown in Fig. 6(a), is reverse biased, at 1 V, to match the biasing conditions of the TFET. For gate voltages(V_{GS}) beyond 4 V, the thin gate dielectric starts to leak. From this curve, a minimum subthreshold swing of 240 mV/dec was measured for the gated pn diode [Fig. 6(c)].

Finally, the TFET transfer characteristics were also measured using a constant drain bias of 1 V [Fig. 6(b)]. A maximum current saturation of 57 μA/μm is achieved for a positive V_{DS} of 1 V. From this plot, an On/Off ratio of six orders is estimated. Figure 6(c) highlights the extracted subthreshold swing for the TFET at room temperature, with a minimum of 102 mV/dec. A likely cause for a SS greater than 60 mV/dec is trap-assisted tunneling, a well-known limiting factor in heterostructure TFETs.[33,34] Comparing Figs. 6(a) with 6(b) proves the drastic increase in the interband tunneling current by introducing a thin (7 nm) InGaN layer. The lowest subthreshold swing of the device is more than halved while its threshold voltage is also reduced, while also improving the On/Off ratio by an order. These tunneling current

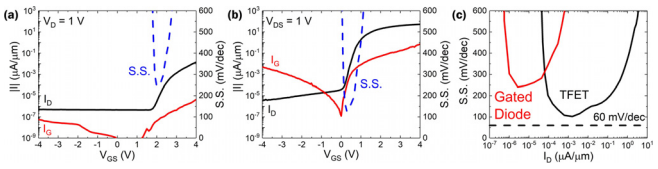

FIG. 6. Transfer characteristics and the extract subthreshold swings for each device. (a) For the gated p-n diode, application of gate voltages greater than 2 V enables a tunneling current. (b) TFET transfer characteristics highlighting the improvements brought about by the InGaN tunnel layer: a reduced threshold voltage while keeping a high On/Off ratio. (c) SS for each device. The gated diode is limited to 240 mV/dec. The SS in the TFET is improved, reaching 102 mV/dec due to the inclusion of the thin InGaN tunnel junction.

densities are about an order of magnitude higher than those predicted by Ameen *et al.*[28] for the given InGaN layer, and likely arise from the threading dislocations.

In order to gain a better understanding of the impact of defects on the performance of the TFET, numerical simulations were carried out using technology computer-aided design (TCAD) simulator Sentaurus (not shown). The details for this can be found in Refs. 25 and 26. It should be noted that the simulation does not take quantization effects in account, which results in an underestimation of the On current for the device. However, it can still offer insight into the expected subthreshold swing for a device with 7 nm InGaN barrier and 27% In composition. At room temperature, the simulated SS minimum is 69 mV/dec. When compared to the experimental value of 102 mV/dec, there is a clear discrepancy. As is stated earlier, a likely cause for this is trap assisted tunneling, which stems from defects at the InGaN/GaN interface. Due to the large lattice mismatch between GaN and InGaN, it is common for defects to be introduced at this interface. Moreover, the growth employed to realize this TFET utilized an interrupt between the InGaN tunnel barrier and the UID channel. Such a technique likely introduced further defects, which contribute to the reduced SS measured compared to simulations.

A TEM study was done on the completed TFET, as shown in Fig. 7(a). This image confirms that the vertical process creates a device with the desired geometry. Upon closer inspection, however, the threading dislocations generated at the UID GaN/InGaN interface are cause for concern. After the growth of the InGaN layer, 5 nm of low temperature UID GaN is grown to prevent decomposition of the InGaN when the substrate temperature is increased. Figure 7(b) shows a close up of this growth interface. The dislocations are found to have formed during the low temperature UID GaN growth. Fortunately, the dislocations do not propagate into the InGaN region, or to the p-GaN source region underneath. However, by acting as conduction paths for the trap assisted carriers at the center of the wire, the dislocations are a possible reason for the experimental current being an order of magnitude higher than theoretical predictions. Another area of concern is the delamination of the Cr/Pt etch masks at the contact edges in Fig. 7(a) due to the high tensile stress in Pt from metal evaporation. However due to the high doping in the top GaN layer, current spreading is sufficient enough that the metal delamination did seem to degrade device performance.

In conclusion, two types of vertical FETs were implemented in GaN. The gated p-n diode showed that strong modulation of the internal charge is possible while preserving the p-n junction characteristics. For the GaN TFET, by adding a 7 nm InGaN layer between the p-type and undoped GaN junction, efficient interband tunneling injection is engineered in reverse bias. This allows the device to achieve saturation currents of 57 μA/μm while reducing the SS to 102 mV/dec. Further reduction in wire diameter and gate oxide thickness, combined with optimization of epitaxial growth of the polarization-induced nitride tunnel junctions, has the potential to enable a SS below the Boltzmann limit and harnesses the very low off currents possible in this unique semiconductor platform.

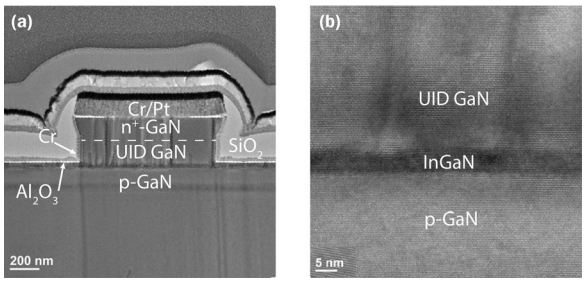

FIG. 7. (a) Wide view TEM of measured TFET. Delamination of etch mask metal at contact edges presents potential for gate to drain shorts. Extended threading dislocations are generated at the InGaN/UID GaN interface but do not extend into the InGaN layer. (b) Zoomed in TEM image of the InGaN tunnel junction showing that the InGaN is 7 nm thick.

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